Switching Behaviour of GaN-based Power Converter subject to Current-Collapse Effect in Double-Pulse Test

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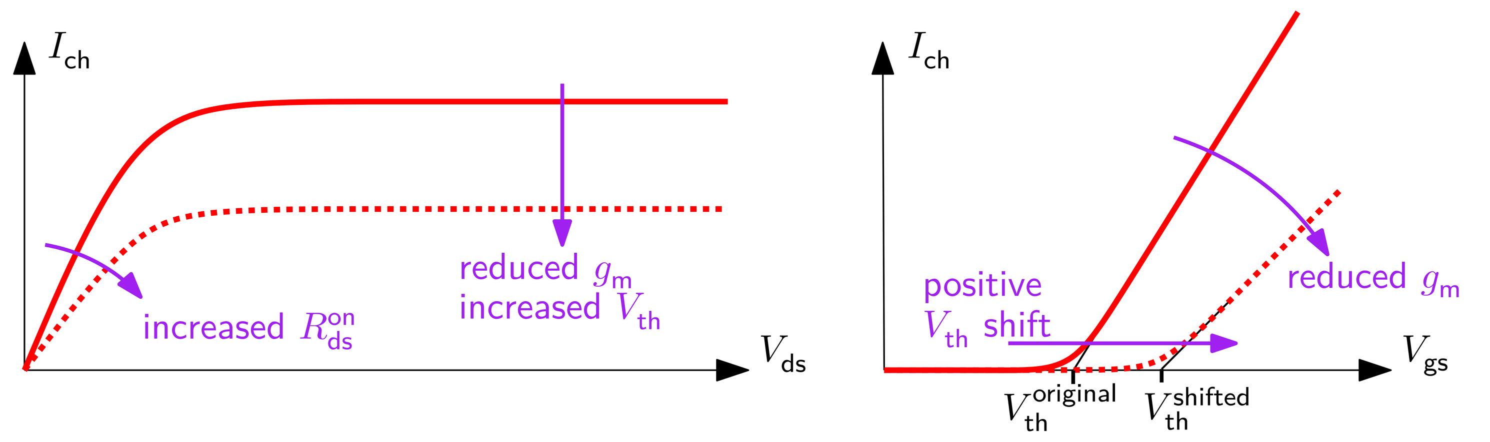
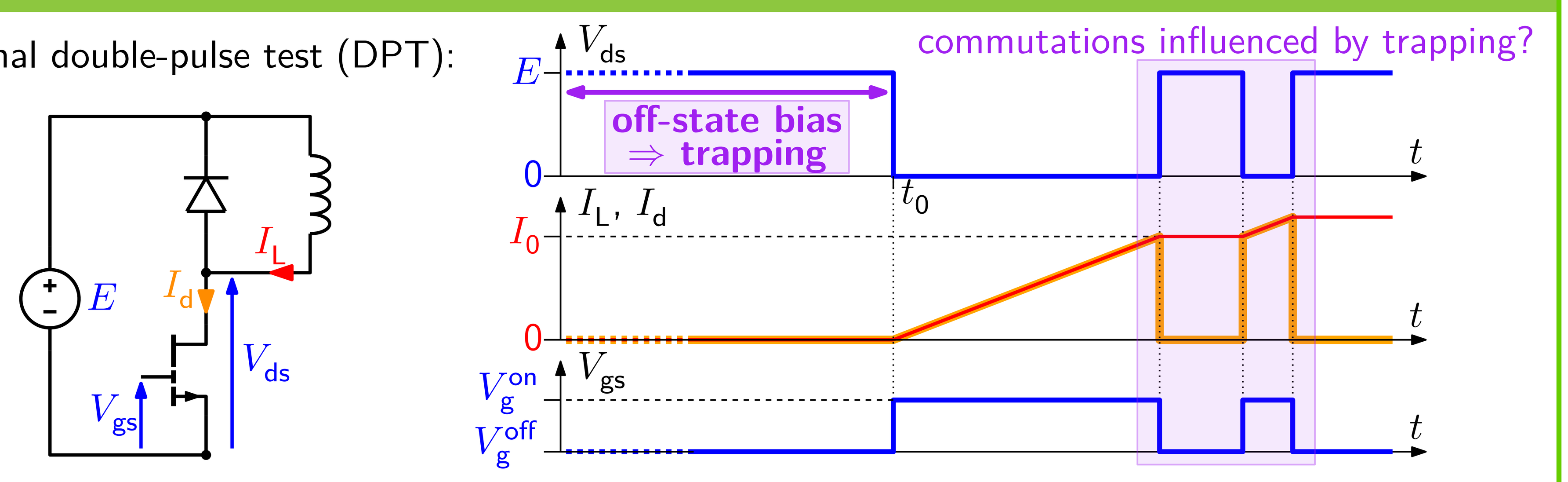
Motivation and Objectives

GaN trapping effect: not only dynamic R_{ds}^{on}

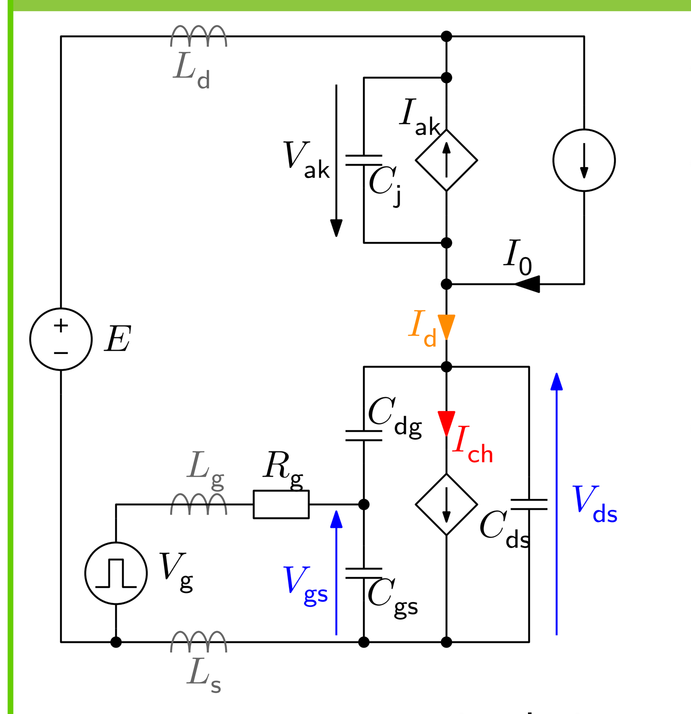


Conventional double-pulse test (DPT):



How does current collapse influence switching behaviour? ⇒ Theoretical analysis on switching waveforms and circuit stability – Experimental evaluation on modified DPT bench

Influence on Switching Waveforms



- simplified model (no $L_{d/g/s}$): $-\frac{dV_{ds}}{dt} = \frac{I_{ch} - I_0}{C_{ds} + C_{dg} + C_j}$ ← ΔI_{ch}
- at Miller plateau, if any (constant $C_{gs/ds/dg}$):

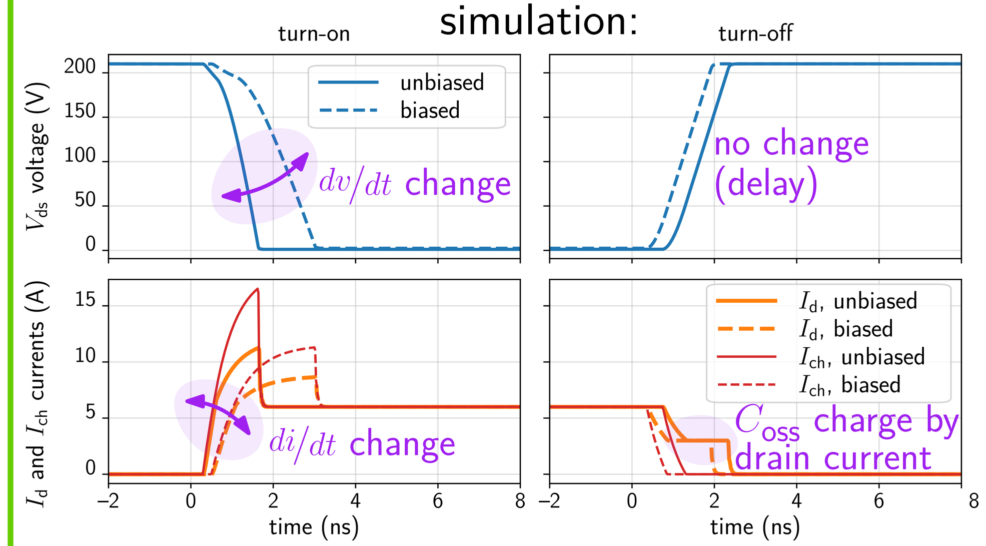
$$I_{ch} = I_0 - \frac{V_{gs} - V_g}{R_g}\left(1 + \frac{C_{ds} + C_j}{C_{dg}}\right) \quad \longleftarrow \text{ from circuit}$$
$$= g_m(V_{gs} - V_{th}) \quad \longleftarrow \text{ transfer characteristic}$$

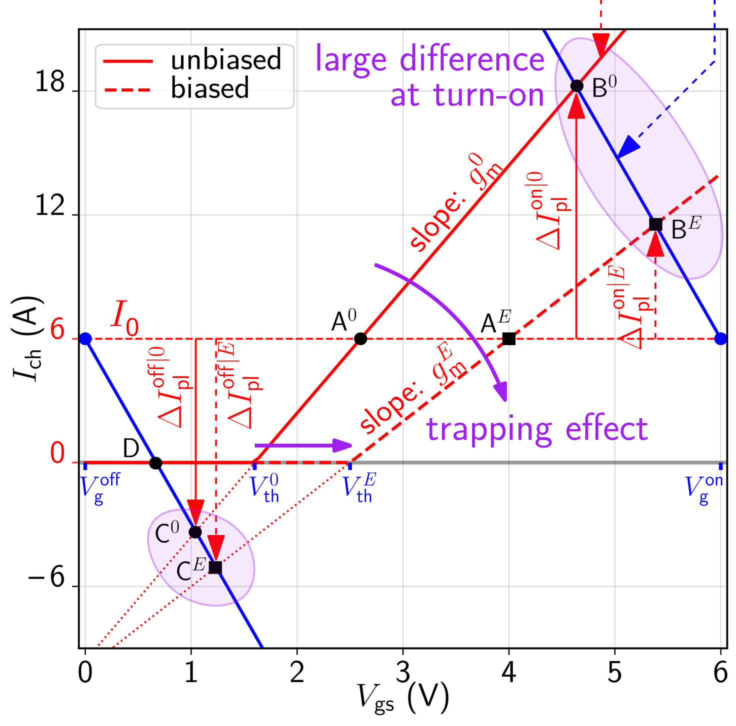
- thus, $-\frac{dV_{ds}}{dt} = \frac{g_m(V_g - V_{th}) - I_0}{g_m R_g C_{dg} + C_{ds} + C_{dg} + C_j} = f(g_m, V_{th})$

at turn-on: $\frac{\partial f}{\partial g_m} > 0$ and $\frac{\partial f}{\partial V_{th}} < 0$

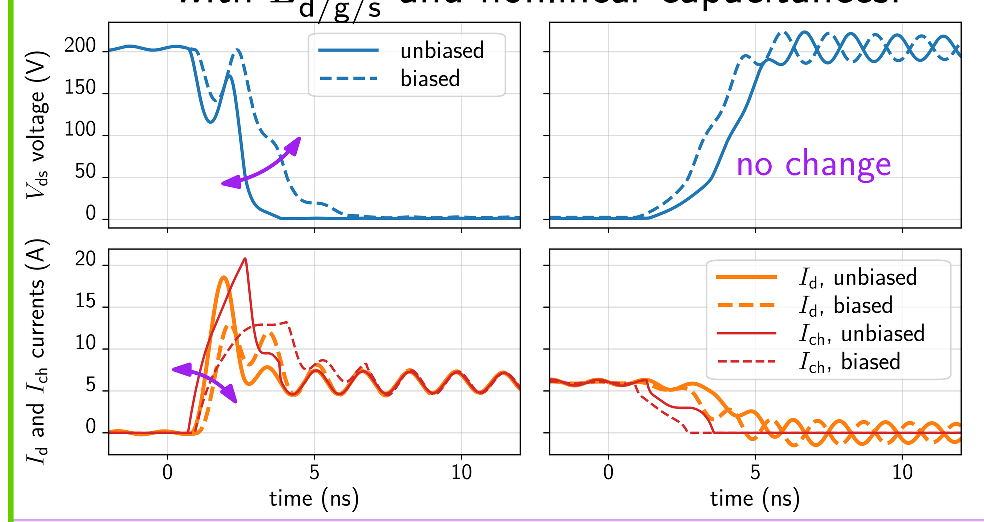
⇒ expected impact on switching speed

simulation:

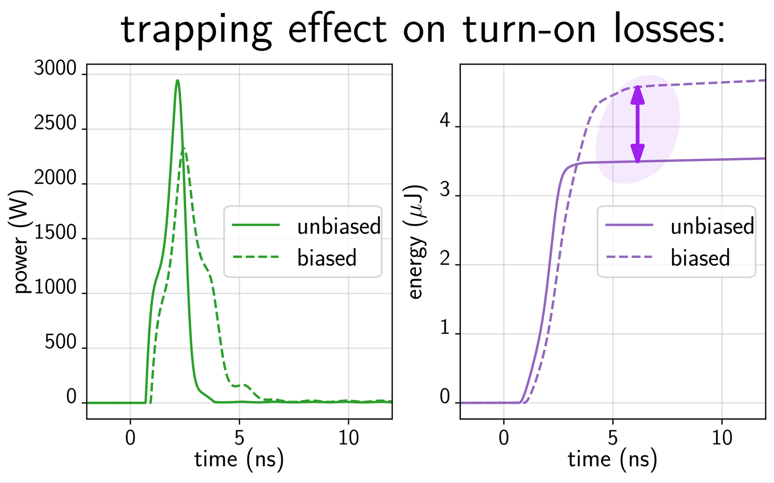




with $L_{d/g/s}$ and nonlinear capacitances:

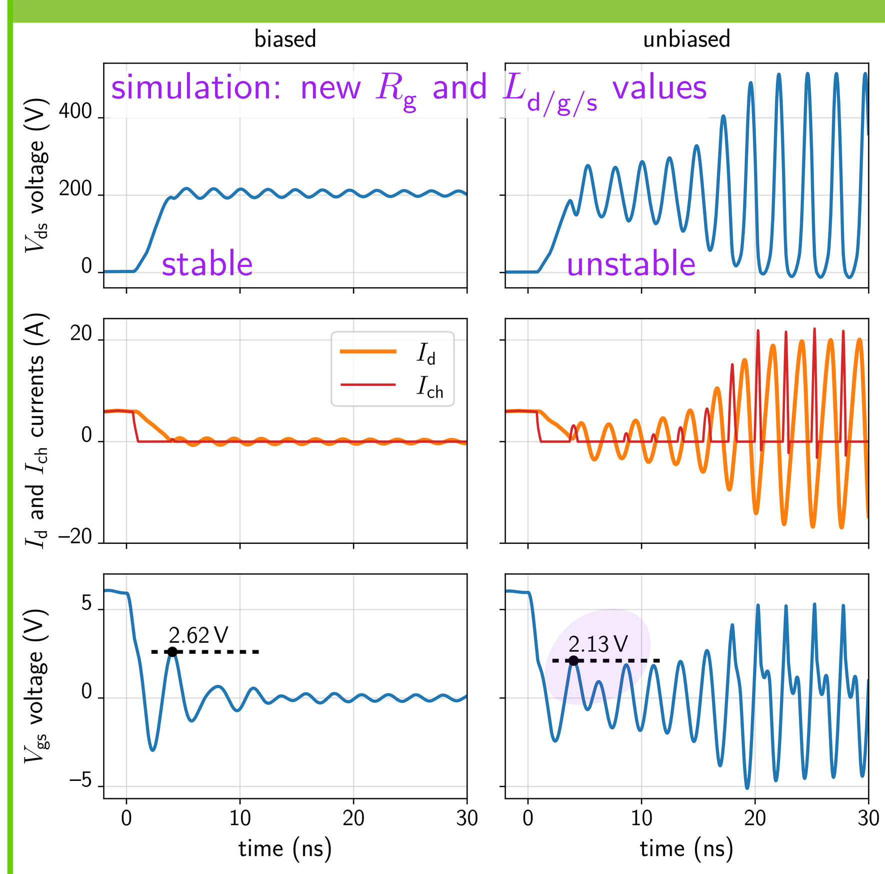


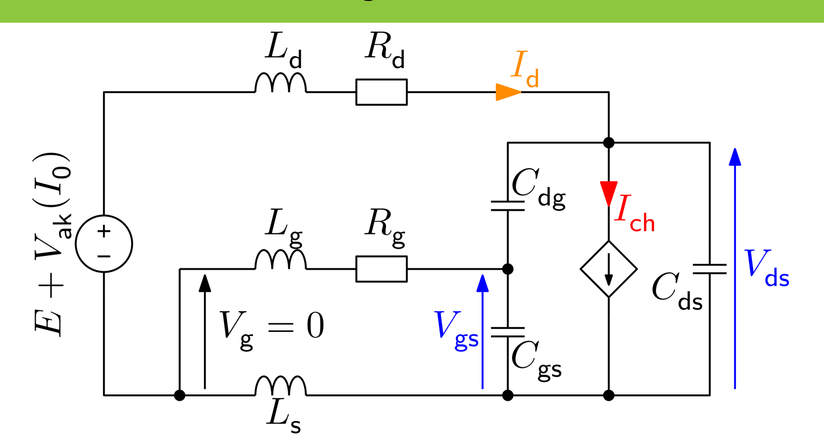
trapping effect on turn-on losses:



${di}/{dt}$, ${dv}/{dt}$ and losses impact at turn-on. Seems no effect at turn-off, but…

Influence on Circuit Stability





I_{ch} small-signal excitation yields V_{gs} response:

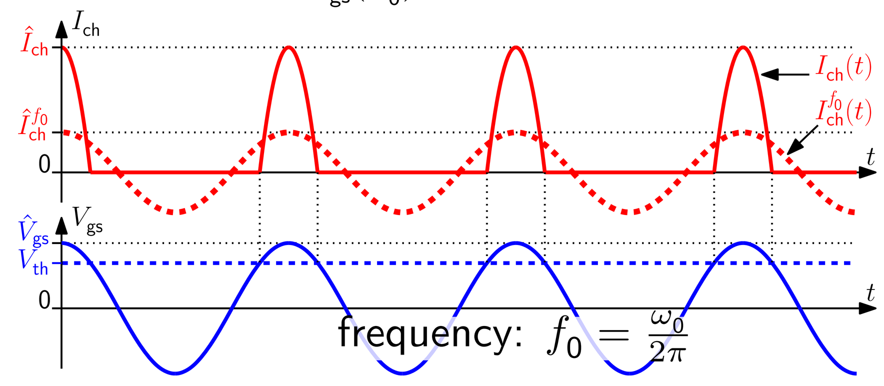
$$V_{gs}(\omega) = Z_t(\omega) I_{ch}(\omega) = \frac{I_{ch}(\omega)}{Y_t(\omega)}$$

introducing equivalent transconductance:

$$I_{ch}(t) = g_{eq} V_{gs}(t)$$

sustained oscillations are obtained at ω_0 when:

$$g_{eq}^{lim} = \frac{I_{ch}(\omega_0)}{V_{gs}(\omega_0)} = Y_t(\omega_0) \in \mathbb{R}_+$$

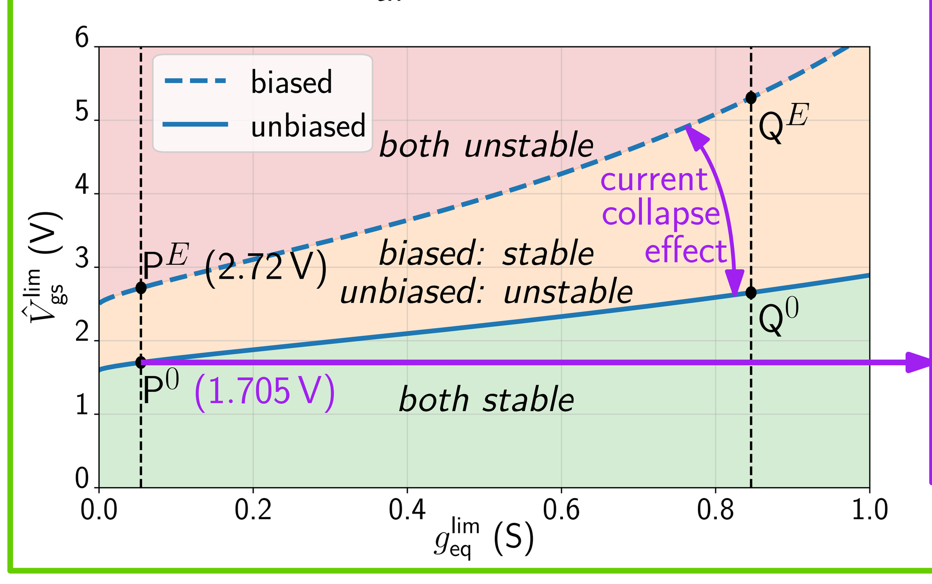


- large-signal non-sinusoidal I_{ch} approximated to its fundamental harmonic:

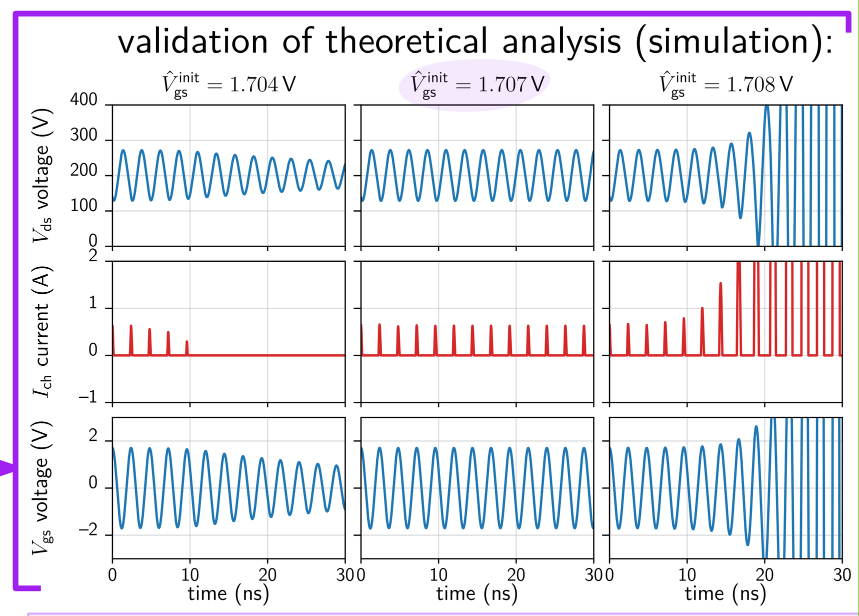
$$g_{eq}^{lim} = \frac{\hat{I}_{ch}^{f_0}}{\hat{V}_{gs}^{lim}} = \frac{g_m}{\pi}\left(\arccos X - X\sqrt{1 - X^2}\right)$$

with $X = {V_{th}}/{\hat{V}_{gs}^{lim}}$, defining maximum gate ringing amplitude $\hat{V}_{gs}^{lim}$ before instability

- $\hat{V}_{gs}^{lim}$ computed for a given circuit g_{eq}^{lim} and device g_m and V_{th} (influenced by trapping):



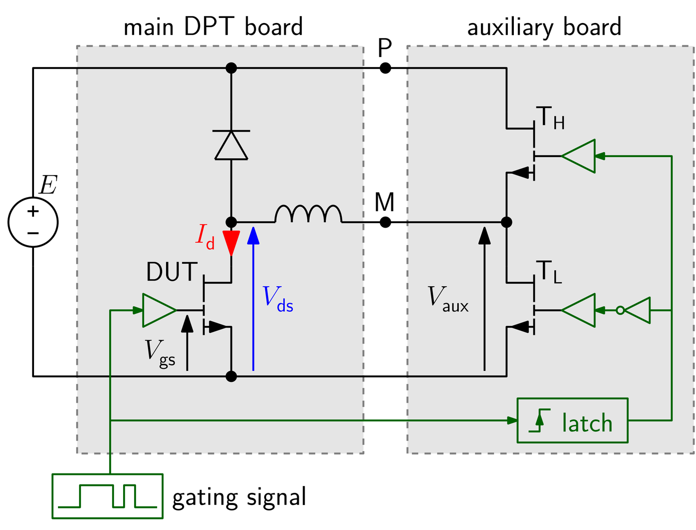
validation of theoretical analysis (simulation):



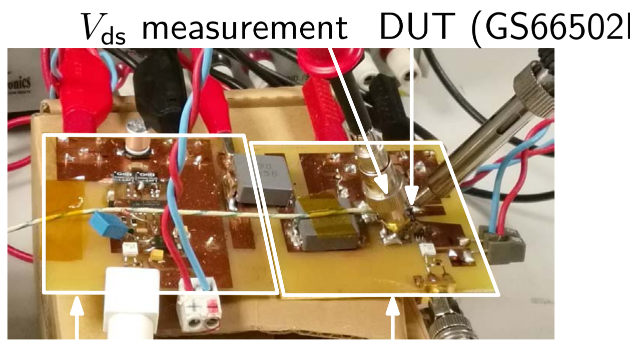
impact on immunity margin to instability

Experimental Results

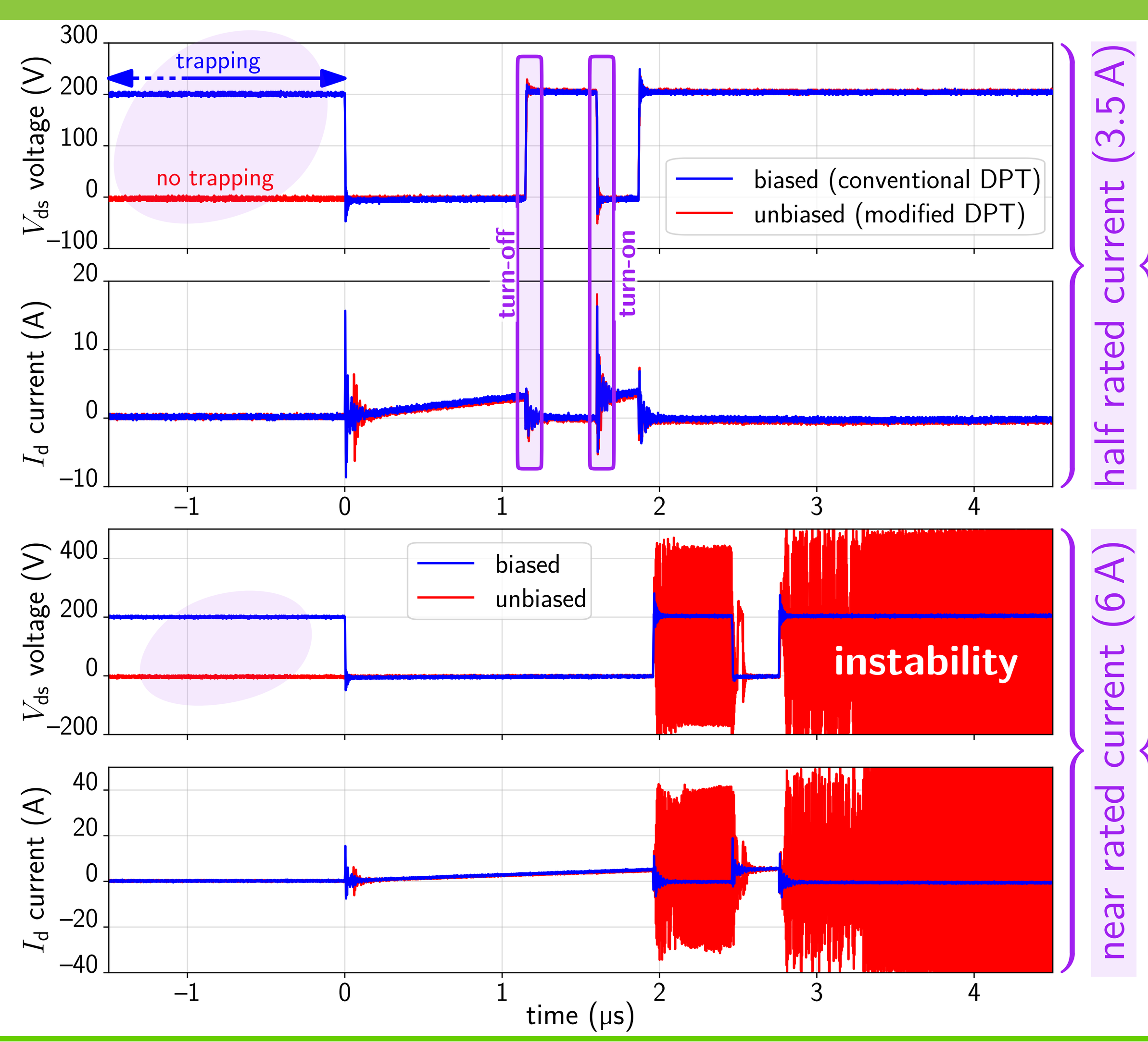
modified DPT setup:
allows zero bias before test

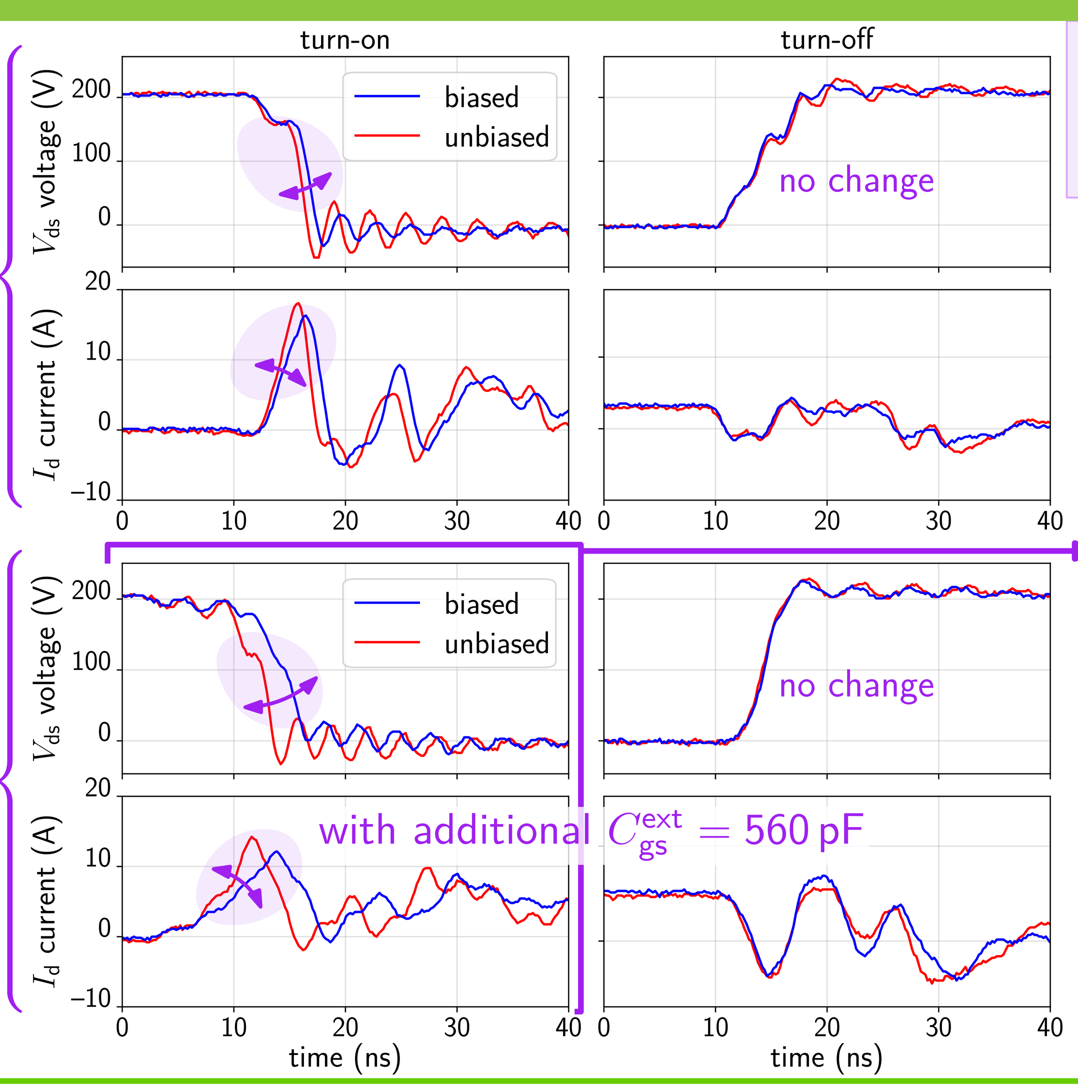


V_{ds} measurement DUT (GS66502B)

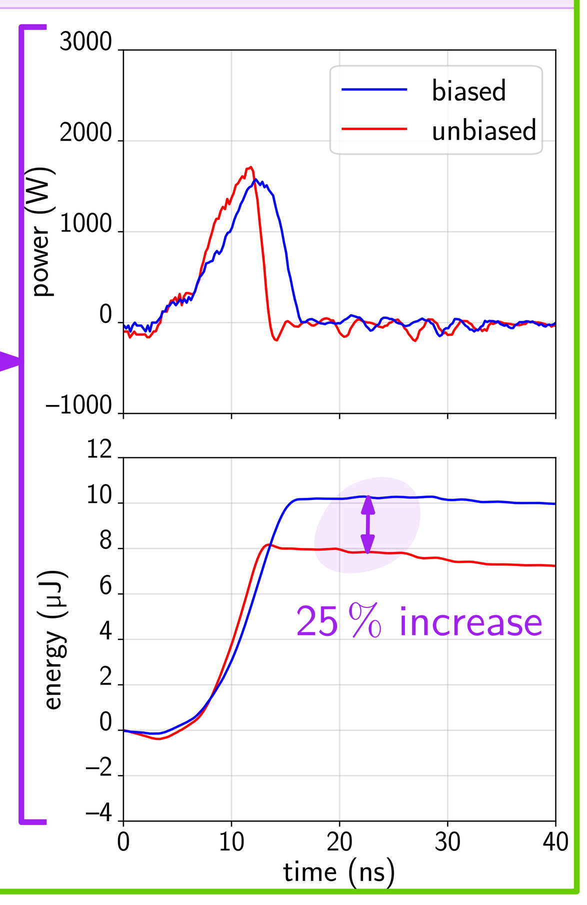


auxiliary board main board





measurements confirm current collapse influence on switching waveforms and circuit stability



Conclusion

- trapping effect **influences turn-on switching waveforms**
- possible impact on **EMC and switching losses**
- similar turn-off waveforms but current collapse impacts **immunity to gate instability**
- **conventional DPT can be misleading for losses estimation, reliability assessment, or comparison with simulations** due to pre-bias trapping that might not reflect actual use
- **modified DPT allows experimental evaluation** of current-collapse influence

Acknowledgement

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